Our Ref. No.: 004006.P001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Lee McBryde,

Serial No.: 09/882,471

Filing Date: June 14, 2001

For: **DATA MANAGEMENT ARCHITECTURE**

Examiner: Mujtaba M. Chaudry

Art Unit: 2133

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicant requests review of final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reasons stated on the attached sheets.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN

Dated: September 6, 2005

By: _____
Eric S. Hyman, Reg. No. 30,139

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class Mail , With Sufficient Postage, In An Envelope Addressed To: Commissioner For Patents, P.O. Box 1340, Alexandria, VA 22313-1450.

Kenneth Schmidt — September 6, 2005

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicant requests review of the final rejection in the above-identified application based upon the following.

In a final Office Action mailed April 5, 2005, claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by DeKoning et al. In support of this rejection, in the sentence bridging pages 3 and 4 of the Action, the Examiner states:

"In particular, DeKoning teaches (Figs. 1 and 2) the XOR engine (62) coupled to the memory controller (60), which is analogous to the hosts/network interface of the present application." (emphasis added)

Claim 1 of the application recites, with reference numbers added, "XOR engine (33), a host network interface (31) coupled to said XOR engine . . ., a cache (35) coupled to said XOR engine (33) . . ."

For the convenience of the reviewers, attached hereto is a sheet showing prior art Figs. 1 and 2 and Fig. 3 of the invention.

As clearly shown in the attached figures, in the prior art, memory controller (60) is coupled to PCI bus (28). This is to be contrasted with Applicant's invention as shown in Fig. 3, wherein XOR engine (33) is shown as being coupled to hosts/network interface (31). If there is any element in the prior art which can be said to be analogous to hosts/network interface (31), it is host interface (16) of the prior art.

Notwithstanding that the prior art shows that host interface (16) is coupled to host device (31), the Examiner contends that memory controller (60) is analogous to Applicant's hosts/network interface (31) such that the claim limitation of the XOR engine being coupled to the host network interface is met by the prior art.

However, it is easily demonstrated that DeKoning's memory controller (60) is not analogous to hosts/network interface (31). As explained at page 4 of the application, at paragraph [0027] hosts/network interface (31) is a communications interface to a host computer or network of computers. This is, of course, consistent with the ordinary English language meaning of a hosts/network interface and is consistent with the description of hosts/network interface (31) in Fig. 3, which is shown as being for coupling to host/network. Clearly, the reference to host in Fig. 3 corresponds to the reference to DeKoning's host device (31) in prior art Figs. 1 and 2. Thus, on its face, it should be apparent that the prior art memory controller (60) is not analogous to Applicant's host/network interface (31). Further proof that memory controller (60) is not analogous to hosts/network interface (31) is provided by the Examiner at page 3 of the Action, wherein it is stated "the RPA memory controller (60) controls (1) a flow of data between the system bus (28), the RPA memory (22), and the intermediate parity buffer (64), and (2) the operation of XOR engine (62). That is, DeKoning's memory controller (60) operates exactly as its name implies, i.e., it controls the flow of data to and from a memory. This is to contrast with the operation of Applicant's hosts/network interface (31), which is described in the application in one embodiment as translating and decoding fiber channel commands into data and non-data commands precisely the type of operations expected of a host/network interface. See paragraph [0027] at page

5 of the application.

In view of the foregoing, Applicant submits that it has been demonstrated that the Examiner's rejection is clearly erroneous, in that it is based upon an erroneous conclusion that the memory controller (60) is analogous to Applicant's hosts/network interface (31).

Applicant notes that independent claims 6, 7, 8, 12 and 13 contain additional limitations the Examiner has failed to consider, which will be fully explained should it become necessary to file an appeal brief.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN

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